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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/598,173	06/21/2000	Bernd Moller	2789-17	6943

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Nixon & Vanderhye PC
8th Floor
1100 North Glebe Rd
Arlington, VA 22201-4714

EXAMINER	
PATEL, NITIN C	
ART UNIT	PAPER NUMBER
2185	10

DATE MAILED: 08/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/598,173	MOLLER ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *7 and 23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-22 and 24-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This is in responsive to amendment filed on June 17, 2003.

2. Claims 7, and 23 have been cancelled.

3. Claims 1 – 6, 8 – 22, and 24 – 30 are presented for the examination.

Claim Objections

4. Claims 8, and 24 objected to because of the following informalities: The dependency of claims 8, and 24, are on claim 7, and 23 respectively which are canceled as per the amendment filed on June 17, 2003. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1 – 2, 6, 8 – 9, 11 – 18, 22, 24 – 25, and 27 – 30, are rejected under 35 U.S.C. 103(a) as being unpatentable over DeRoo et al. [hereinafter as DeRoo], US Patent 6,009,495 [cited in previous office action], and further in view of Alexander et al. [hereinafter as Alexander], US Patent 5,363,334.

7. As to claims 1, and 17, DeRoo teaches the system and method to provide a non-volatile sector in a programmable memory [EEPROM] from inadvertent erasure by intercepting data-write commands to the protected sector of the memory and erase software commands sent by the

CPU host to the EEPROM with preventing the write control signal to the memory to be asserted when address of the data access requested by the CPU is in the protected area of the memory [col. 3, lines 5 – 10, and 23 – 40]. However, DeRoo does not disclose the mechanism to protect the data stored initially in protected part of memory from any subsequent writing into protected part by irreversible blocking. In summary, DeRoo does not teach the technique to protect the data of protected part of memory other than predetermined address range.

Alexander teaches system and method of write protection security for memory device with security scheme defines the first block to be write protected, and also number of contiguous blocks to be write protected commencing with that security start block by storing the bits in registers with set of configuration fuses that act as lockout [col. 2, lines 30 – 48, col. 7, lines 1 – 38] which prevent reassure and rewriting of data in the selected memory blocks.

It would have been an obvious to one of an ordinary skill in art at the time of invention to combine the teachings of DeRoo and Alexander because both are related to write protection of data in memory in protected part of memory and Alexander's teachings of security scheme provide security to data storage cells against overwriting or erasure over which write protection is to be provided [col. 2, lines 55 – 63, col. 3, lines 1 – 13].

8. As to claims 2, and 18, Alexander discloses that processor stores permanent start addresses that are necessarily called upon start-up of the processor [it is inherent to the start or boot up of processor to call upon the start address], where at least one of the start addresses points to the protected part of the memory [col. 2, lines 30 – 43, col. 6, lines 55 – 67].

9. As to claims 6, and 22, DeRoo discloses plurality of memory devices, one of which comprises the protected part [fig. 27].

10. As to claims 8, and 24, Alexander discloses that writing data into protected part [block] via a write line, and sending a signal to the protected part [block] the write line is permanently interrupted [whenever write operation is attempted to the protected block, a compare step is performed, and if it is determined that the write address of the write operation is within protected [secured] area then write is aborted][col. 2, lines 44 – 48].

11. As to claims 9, and 25, Alexander discloses the use of a fusible link to permanently interrupt a line, thus causing an open [col. 7, lines 16 – 22].

12. As to claim 11, and 27, Alexander discloses the EEPROM and flash memory [OTP] [col. 1, lines 31 – 33].

13. As to claims 12, and 28, it is inherent to the assembly process or component mounting on board to have memory chip having electrical contacts for being connected to the circuit board.

14. As to claims 13, and 29, it is inherent to provide electrical contacts to the ball grid array [BGA] components.

15. As to claims 14 – 16, and 30, DeRoo discloses devices in need of substantially described claimed invention [col. 2, lines 19 – 21].

Claim Rejections - 35 USC § 103

16. Claims 10, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeRoo et al. [hereinafter as DeRoo], US Patent 6,009,495 [cited in previous office action], and further in view of Alexander et al. [hereinafter as Alexander], US Patent 5,363,334 as applied to claims 1, and 17 above, and further in view of Kynett et al. [hereinafter as Kynett] [cited in previous office action], US Patent 5 546,561.

17. As to claims 10, and 26, DeRoo and Alexander disclose the claimed invention substantially. However, DeRoo and Alexander do not teach write protection by implementing a finite state machine. In summary, neither DeRoo nor Alexander discloses a finite state machine.

Kynett discloses a finite state machine defining a state, which protects said protected part from being overwritten into within a non-volatile semiconductor memory [col. 6, lines 1 – 7]. It would have been an obvious to one of an ordinary skill in art at the time of invention was made to combine the cited references because all them are related to controlling write and read of memory and teachings of Kynett state machine would simplify the process by deceasing the system throughput [col. 2, lines 47 – 57].

Claim Rejections - 35 USC § 103

18. Claims 3 – 5, and 19 - 21 rejected under 35 U.S.C. 103(a) as being unpatentable over DeRoo et al. [hereinafter as DeRoo], US Patent 6,009,495 [cited in previous office action], and further in view of Alexander et al. [hereinafter as Alexander], US Patent 5,363,334 as applied to claims 1, and 17 above, and further in view of Davis et al. [hereinafter as Davis] [cited in previous office action], US Patent 6,401,208 B2.

19. As to claims 3, and 19, DeRoo and Alexander disclose the claimed invention substantially. However, they do not disclose the program routine from protected part upon start-up comprises checking for changes in at least a part of the data contained in said second part. In summary, neither DeRoo nor Alexander discloses the program routine upon start-up to check for changes in at least a part of the data contained in second part.

Davis discloses authenticating software code, before permitting host processor to execute the software code [col. 2, lines 26 – 28].

It would have been an obvious to one of an ordinary skill in art at the time of invention was made to combine the cited references because all of them are related to memory access and teachings of Davis would have provided ability to check if the BIOS of the system had been changed in anyway upon startup although the boot block is protected from being written into the BIOS is susceptible to unauthorized changes which allows to identify BIOS corruption and take appropriate actions.

20. As to claims 4, and 20, Davis discloses calculating a characteristic parameter for data being checked for changes, and comparing said characteristic parameter with a value in said second part [fig. 6B].

21. As to claims 5, and 21, Davis discloses said characteristic parameter is a checksum [fig. 6B].

22. Applicant's arguments with respect to claims 1-6, 8-22, and 24-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

23. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 703-305-3994. The examiner can normally be reached on 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Nitin C. Patel
August 5, 2003

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100